

WHAT IS CLAIMED IS:

1           1. A thin film transistor array substrate comprising:  
2           an insulating substrate;  
3           a first metallic pattern formed on said insulting substrate;  
4           an insulating film provided on said first metallic pattern;  
5           a semiconductor pattern provided on said insulating film;  
6           and  
7           a second metallic pattern provided on said semiconductor  
8           pattern;  
9           wherein said second metallic pattern is surrounded by said  
10          semiconductor pattern.

1           2. The thin film transistor array substrate according to claim  
2           1, wherein at the source electrode part in a pixel region, a part of the  
3           semiconductor pattern surrounding the source electrode exists only on  
4           the first metallic pattern.

1           3. A thin film transistor array substrate comprising:  
2           an insulating substrate;  
3           a gate line formed on said insulating substrate;  
4           a gate insulating film provided on said gate line;  
5           a semiconductor layer provided on said gate insulating film;  
6           a source line, a source electrode and a drain electrode  
7           provided on said semiconductor layer;  
8           and  
9           a pixel electrode formed on said drain electrode;

10            wherein said source line, said source electrode and said  
11 drain electrode are surrounded by said semiconductor layer;

12            wherein said pixel electrode is directly in contact with at least  
13 a portion of said drain electrode.

1            4. A thin film transistor array substrate comprising:

2            an insulating substrate;

3            a gate line formed on said insulating substrate;

4            a gate insulating film provided on said gate line;

5            a semiconductor layer provided on said gate insulating film;

6            a source line, a source electrode and a drain electrode  
7 provided on said semiconductor layer;

8            an inter-layer insulating film formed on said source line, said  
9 source electrode and said drain electrode; and

10           a pixel electrode formed on said inter-layer insulating film;

11           wherein said source line, said source electrode and said  
12 drain electrode are surrounded by said semiconductor layer;

13           wherein said inter-layer insulating film is provided with a  
14 first contact hole, a second contact hole and a third contact hole, said  
15 first contact hole penetrating said inter-layer insulating film to reach  
16 said drain electrode, said second contact hole extending to said source  
17 line through said inter-layer insulating film, said third contact hole  
18 extending to said gate line through said gate insulating film and said  
19 inter-layer insulating film; and

20           wherein said first contact hole, said second contact hole and  
21 said third contact hole are covered with a pattern made of a material of  
22 said pixel electrode.

1           5. The thin film transistor array substrate according to claim  
2 4, wherein at the source electrode part in a pixel region, a part of the  
3 semiconductor pattern surrounding the source electrode exists only on  
4 the gate line.

1           6. Method for manufacturing a thin film transistor array  
2 substrate comprising steps of:

3           a first photolithography and etching step for forming a gate  
4 line;

5           depositing a gate insulating film, a semiconductor film, an  
6 ohmic contact film and a first metallic thin film;

7           a second photolithography step for forming a resist pattern of  
8 a source line, a source electrode, and a drain electrode;

9           forming a region of said resist pattern serving as a  
10 semiconductor active layer in the thin film transistor in such a manner  
11 that thickness of said resist pattern in at least said region serving as a  
12 semiconductor active layer is smaller than that in said source line, said  
13 source electrode and said drain electrode in the second  
14 photolithography process after depositing a second metallic film;

15           etching said second metallic film to form the source line, the  
16 source electrode and the drain electrode;

17           removing the resist in the region serving as a semiconductor  
18 active layer and etching said second metallic film to remove said second  
19 metallic film on said region serving as a semiconductor active layer,  
20 removing said ohmic contact film on said region serving as a  
21 semiconductor active layer;

22           a third photolithography and etching step of patterning the

23 gate insulating film for forming a contact hole extending to the gate line;  
24 depositing a conducting film; and  
25 a fourth photolithography and etching step of forming a pixel  
26 electrode in such a manner that said pixel electrode is connected with  
27 said drain electrode.

1 7. Method for manufacturing a thin film transistor array  
2 substrate comprising steps of:

3 a first photolithography and etching step for forming a gate  
4 line;

5 depositing a gate insulating film, a semiconductor film, an  
6 ohmic contact film and a first metallic thin film;

7 a second photolithography step for forming a resist pattern of  
8 a source line, a source electrode, and a drain electrode;

9 forming a region of said resist pattern serving as a  
10 semiconductor active layer in the thin film transistor in such a manner  
11 that thickness of said resist pattern in at least said region serving as a  
12 semiconductor active layer is smaller than that in said source line, said  
13 source electrode and said drain electrode in the second  
14 photolithography process after depositing a second metallic film;

15 etching said second metallic film to form the source line, the  
16 source electrode and the drain electrode;

17 removing the resist in the region serving as a semiconductor  
18 active layer and etching said second metallic film to remove said second  
19 metallic film on said region serving as a semiconductor active layer,  
20 removing said ohmic contact film on said region serving as a  
21 semiconductor active layer;

22           a third photolithography and etching step of patterning the  
23 gate insulating film for forming a contact hole extending to the gate line;  
24           depositing a conducting film; and  
25           a fourth photolithography and etching step of forming a pixel  
26 electrode in such a manner that said pixel electrode is connected with  
27 said drain electrode, forming a source terminal in such a manner that  
28 said source terminal is connected with said source line, forming a gate  
29 terminal in such a manner that said gate terminal is connected with said  
30 gate line.

1           8. Method for manufacturing a thin film transistor array  
2 substrate comprising steps of:

3           a first photolithography and etching step for forming a gate  
4 line;

5           depositing a gate insulating film, a semiconductor film, an  
6 ohmic contact film and a first metallic thin film;

7           a second photolithography step for forming a resist pattern of  
8 a source line, a source electrode, and a drain electrode;

9           forming a region of said resist pattern serving as a  
10 semiconductor active layer in the thin film transistor in such a manner  
11 that thickness of said resist pattern in at least said region serving as a  
12 semiconductor active layer is smaller than that in said source line, said  
13 source electrode and said drain electrode in the second  
14 photolithography process after depositing a second metallic film;

15           etching said second metallic film to form the source line, the  
16 source electrode and the drain electrode;

17           thinning the resist to remove the resist only in the region

18 serving as a semiconductor active layer and etching said second metallic  
19 film to remove said second metallic film on said region serving as a  
20 semiconductor active layer, removing said ohmic contact film on said  
21 region serving as a semiconductor active layer;

22 depositing an inter-layer insulating film;

23 a third photolithography and etching step of patterning said  
24 gate insulating film and said inter-layer insulating film to form a first  
25 contact hole extending to said drain electrode, a second contact hole  
26 extending to said source line and a third contact hole extending to said  
27 gate line;

28 depositing a conducting film; and

29 a fourth photolithography and etching step of forming a pixel  
30 electrode in such a manner that said pixel electrode is connected with  
31 said drain electrode via said first contact hole, forming a source terminal  
32 in such a manner that said source terminal is connected with said  
33 source line via said second contact hole, forming a gate terminal in such  
34 a manner that said gate terminal is connected with said gate line via said  
35 third contact hole.

1 9. Method for manufacturing a thin film transistor array  
2 substrate comprising steps of:

3 a first photolithography and etching step for forming a gate  
4 line and a conversion line for a source line;

5 depositing a gate insulating film, a semiconductor film, an  
6 ohmic contact film and a first metallic thin film;

7 a second photolithography step for forming a resist pattern of  
8 a source line, a source electrode, and a drain electrode;

9           forming a region of said resist pattern serving as a  
10 semiconductor active layer in the thin film transistor in such a manner  
11 that thickness of said resist pattern in at least said region serving as a  
12 semiconductor active layer is smaller than that in said source line, said  
13 source electrode and said drain electrode in the second  
14 photolithography process after depositing a second metallic film;

15           etching said second metallic film to form the source line, the  
16 source electrode and the drain electrode;

17           removing the resist in the region serving as a semiconductor  
18 active layer and etching said second metallic film to remove said second  
19 metallic film on said region serving as a semiconductor active layer,  
20 removing said ohmic contact film on said region serving as a  
21 semiconductor active layer;

22           a third photolithography and etching step of patterning said  
23 gate insulating film to form a first contact hole extending to said drain  
24 electrode, a second contact hole extending to said source line, a third  
25 contact hole extending to said gate line, a fourth contact hole extending  
26 to gate line material of said conversion line and a fifth contact hole  
27 extending to the source line;

28           depositing a conducting film; and

29           a fourth photolithography and etching step of forming a pixel  
30 electrode in such a manner that said pixel electrode is connected with  
31 said drain electrode via said first contact hole, forming a source terminal  
32 in such a manner that said source terminal is connected with said  
33 source line via said second, fourth and fifth contact hole, forming a gate  
34 terminal in such a manner that said gate terminal is connected with said  
35 gate line via said third contact hole.

1                   10. Method for manufacturing a thin film transistor array  
2 substrate comprising steps of:  
3                   a first photolithography and etching step for forming a gate  
4 line and a conversion line for a source line formed of a first metallic film;  
5                   depositing a gate insulating film, a semiconductor film, an  
6 ohmic contact film and a first metallic thin film;  
7                   a second photolithography step for forming a resist pattern of  
8 a source line, a source electrode, and a drain electrode;  
9                   forming a region of said resist pattern serving as a  
10 semiconductor active layer in the thin film transistor in such a manner  
11 that thickness of said resist pattern in at least said region serving as a  
12 semiconductor active layer is smaller than that in said source line, said  
13 source electrode and said drain electrode in the second  
14 photolithography process after depositing a second metallic film;  
15                   etching said second metallic film to form the source line, the  
16 source electrode and the drain electrode;  
17                   removing the resist in the region serving as a semiconductor  
18 active layer and etching said second metallic film to remove said second  
19 metallic film on said region serving as a semiconductor active layer,  
20 removing said ohmic contact film on said region serving as a  
21 semiconductor active layer;  
22                   depositing an inter-layer insulating film;  
23                   a third photolithography and etching step of patterning said  
24 gate insulating film and said inter-layer insulating film to form a first  
25 contact hole extending to said drain electrode, a second contact hole  
26 extending to said source line, a third contact hole extending to said gate  
27 line, a fourth contact hole extending to the first metallic film of said



28 conversion line for the source line and a fifth contact hole extending to  
29 said second metallic film;

30 depositing a conducting film; and

31 a fourth photolithography and etching step of forming a pixel  
32 electrode in such a manner that said pixel electrode is connected with  
33 said drain electrode via said first contact hole, forming a source terminal  
34 in such a manner that said source terminal is connected with said  
35 source line via said second, fourth and fifth contact hole, forming a gate  
36 terminal in such a manner that said gate terminal is connected with said  
37 gate line via said third contact hole.

1 11. A thin film transistor array for a liquid crystal display  
2 comprising:

3 a gate line/gate electrode comprising a transparent  
4 conductive layer and a metallic layer provided on said transparent  
5 conductive layer;

6 a pixel electrode defined by the same transparent conductive  
7 layer as said transparent conductive layer of said gate line/gate  
8 electrode; and

9 retaining capacitance electrode formed of the same material  
10 for an electrode as that for a source line, said retaining capacitance  
11 electrode being connected with said pixel electrode;

12 wherein said metallic layer provided on said gate line/gate  
13 electrode is removed from in a part serving as said pixel electrode.

1 12. A thin film transistor array for a liquid crystal display  
2 comprising:

3 a gate line/gate electrode and a common line, both of which  
4 comprise a transparent conductive layer and a metallic layer provided  
5 on said transparent conductive layer;

6 a pixel electrode defined by the same transparent conductive  
7 layer as said transparent conductive layer of said gate line/gate  
8 electrode; and

9 a retaining capacitance electrode formed of the same material  
10 for an electrode as that for a source line, said retaining capacitance  
11 being connected with pixel electrode;

12 wherein said metallic layer provided on said gate line/gate  
13 electrode is removed from in a part serving as said pixel electrode.

1 13. A thin film transistor array for a liquid crystal display  
2 comprising:

3 a gate line/gate electrode comprising a transparent  
4 conductive layer and a metallic layer provided on said transparent  
5 conductive layer;

6 a pixel electrode defined by the same transparent conductive  
7 layer as said transparent conductive layer of said gate line/gate  
8 electrode; and

9 retaining capacitance electrode formed of the same material  
10 for an electrode as that for a source line, said retaining capacitance  
11 electrode being connected with said pixel electrode;

12 wherein said metallic layer provided on said gate line/gate  
13 electrode is removed from in a part serving as said pixel electrode;

14 wherein at least a material for said source line located in a  
15 lowermost layer is the same material as that for said metallic layer of the

16 pixel electrode, when a material for said source line has a multi-layered  
17 structure or said source line per se has a multi-layered structure.

1 14. A thin film transistor array for a liquid crystal display  
2 comprising:

3 a gate line/gate electrode and a common line, both of which  
4 comprise a transparent conductive layer and a metallic layer provided  
5 on said transparent conductive layer;

6 a pixel electrode defined by the same transparent conductive  
7 layer as said transparent conductive layer of said gate line/gate  
8 electrode; and

9 retaining capacitance electrode formed of the same material  
10 for an electrode as that for a source line, said retaining capacitance  
11 electrode being connected with said pixel electrode;

12 wherein said metallic layer provided on said gate line/gate  
13 electrode is removed from in a part serving as said pixel electrode;

14 wherein at least a material for said source line located in a  
15 lowermost layer is the same material as that for said metallic layer of the  
16 pixel electrode, when a material for said source line has a multi-layered  
17 structure or said source line per se has a multi-layered structure

1 15. A thin film transistor array for a liquid crystal display  
2 comprising:

3 a gate line/gate electrode including at least two layers  
4 comprising a metallic layer and a transparent conductive layer, said  
5 metallic layer being formed on said transparent conductive layer;

6 a pixel electrode being formed by a transparent conductive

7 layer which is the same as said transparent conductive layer of said gate  
8 line/gate electrode;

9 a gate insulating film and a semiconductor layer being  
10 formed on at least said gate electrode;

11 source/drain electrodes being formed in such a manner as to  
12 contact with said semiconductor layer;

13 at least an n<sup>+</sup>- Si layer of said semiconductor layer located  
14 between said source/drain electrodes being removed;

15 a retaining capacitance electrode which is formed of a same  
16 layer as that of said source line;

17 a retaining capacitance line including at least two layers  
18 comprising said metallic layer and said transparent conductive layer  
19 simultaneously formed with said gate line, wherein a retaining  
20 capacitance is formed in such a manner that said retaining capacitance  
21 electrode is opposed to said gate line via said gate insulating film;

22 at least said gate insulating film, said semiconductor layer,  
23 and said metallic layer of said pixel electrode being simultaneously  
24 formed with said gate line/gate electrode including at least two layers,  
25 which are located over a light transmitting portion are removed;

26 a part of said semiconductor layer being removed in order  
27 that adjacent source lines are not short-circuited with said  
28 semiconductor layer;

29 said gate insulating film having such a thickness right under  
30 said semiconductor layer is larger than that at any other part of said  
31 gate insulating film.

1 16. A thin film transistor array for a liquid crystal display

2 comprising:

3 a gate line/gate electrode and a common line including two  
4 layers comprising a metallic layer and a transparent conductive layer,  
5 said metallic layer being formed on said transparent conductive layer;

6 a pixel electrode being formed by a transparent conductive  
7 layer which is the same as said transparent conductive layer of said gate  
8 line/gate electrode;

9 a gate insulating film and a semiconductor layer being  
10 formed at least on said gate electrode;

11 a source/drain electrodes being formed in such a manner as  
12 to contact with said semiconductor layer;

13 at least an  $n^+$ -Si layer of said semiconductor layer being  
14 located between said source/drain electrodes is removed;

15 a retaining capacitance electrode, which is formed of a same  
16 layer as said source line, being connected with said pixel electrode;

17 a retaining capacitance line including at least two layers  
18 comprising metallic layer and said transparent conductive layer  
19 simultaneously formed with said gate line, wherein a retaining  
20 capacitance is formed in such a manner that said retaining capacitance  
21 electrode is opposed to said common line via said gate insulating film;

22 at least said gate insulating film, said semiconductor layer,  
23 and said metallic layer of said pixel electrode simultaneously formed  
24 with said gate line/gate electrode including at least two layers, which are  
25 located over a light transmitting portion being removed;

26 a part of said semiconductor layer being removed in order  
27 that adjacent source lines are not short-circuited with said  
28 semiconductor layer;

29           said gate insulating film has such a thickness right under  
30   said semiconductor layer being larger than that at any other part of said  
31   gate insulating film.

1           17. Method for manufacturing a TFT array of liquid crystal  
2   display comprising steps of:

3           depositing a gate electrode/gate line and a pixel electrode,  
4   each of said gate electrode/gate line and said pixel electrode including at  
5   least two layers comprising a transparent conductive layer and metallic  
6   layer provided on said transparent conductive layer, and subsequently  
7   etching said gate electrode/gate line and said pixel electrode using a  
8   photoresist having patterns corresponding to said gate electrode/gate  
9   line and said pixel electrode to form a predetermined patterns;

10          forming a gate insulating film and a semiconductor film;

11          exposing said pixel electrode by etching process using said  
12   photoresist having patterns;

13          removing said metallic layer having at least two layer in said  
14   exposed pixel electrode by etching process; and

15          forming a drain electrode, a source electrode, and a source  
16   line.

1           18. Method for manufacturing a TFT array of liquid crystal  
2   display comprising steps of:

3           depositing a gate electrode/gate line and a pixel electrode,  
4   each of said gate electrode/gate line and said pixel electrode including at  
5   least two layers comprising a transparent conductive layer and metallic  
6   layer provided on said transparent conductive layer, and subsequently

7 etching said gate electrode/gate line and said pixel electrode using a  
8 photoresist having a patterned shape corresponding to said gate  
9 electrode/gate line and said pixel electrode to form a predetermined  
10 patterns;

11 forming a gate insulating film and a semiconductor film;

12 exposing said pixel electrode by etching process using said  
13 photoresist having patterns;

14 forming a metallic layer for a drain electrode, a source  
15 electrode, and a source line;

16 etching said metallic layer using said photoresist having the  
17 the predetermined patterns to form said drain electrode, said source  
18 electrode, and said source line;

19 wherein said metallic layer in said exposed pixel electrode  
20 having at least two layers.

1 19. Method for manufacturing a TFT array of liquid crystal  
2 display comprising steps of:

3 depositing a gate electrode/gate line and a pixel electrode,  
4 each of said gate electrode/gate line and said pixel electrode including at  
5 least two layers comprising a transparent conductive layer and metallic  
6 layer provided on said transparent conductive layer, and subsequently  
7 etching said gate electrode/gate line and said pixel electrode using a  
8 photoresist having a patterned shape corresponding to said gate  
9 electrode/gate line and said pixel electrode to form a predetermined  
10 patterns;

11 forming a gate insulating film and a semiconductor film;

12 forming a region (A) where at least of a portion of said

13 photoresist corresponding to said semiconductor layer to be left has a  
14 thickness being larger than any other part of said photoresist, a region  
15 (C) where at least of a portion of said photoresist corresponding to a light  
16 transmitting part of said pixel electrode to be exposed is removed, and a  
17 region (B) where any parts other than said region (A) and said region (B)  
18 having a thickness smaller than that of said semiconductor layer;

19 etching said semiconductor layer and said gate insulating  
20 film using said photoresist having said thickness in each part to expose  
21 said pixel electrode;

22 removing at least said metallic layer located in upper side of  
23 said two layers in said exposed pixel electrode by etching process;

24 removing said photoresist in said region (B) from upper side  
25 while leaving said photoresist in said region (A);

26 removing said photoresist in any part other than that in said  
27 region (A); and

28 forming a source/drain electrodes.

1 20. Method for manufacturing a TFT array of liquid crystal  
2 display comprising steps of:

3 depositing a gate electrode/gate line, a pixel electrode and a  
4 common line, each of said gate electrode/gate line, said pixel electrode  
5 and said common line including at least two layers comprising a  
6 transparent conductive layer and a metallic layer provided on said  
7 transparent conductive layer;

8 etching said gate electrode/gate line, said pixel electrode and  
9 said common line using a photoresist having a patterned shape  
10 corresponding to said gate electrode/gate line, said pixel electrode and



11 said common line to form a predetermined pattern;  
12 forming a gate insulating film and a semiconductor film;  
13 forming a region (A) where at least of a portion of said  
14 photoresist corresponding to said semiconductor layer to be left has a  
15 thickness being larger than any other part of said photoresist, a region  
16 (C) where at least of a portion of said photoresist corresponding to a light  
17 transmitting part of said pixel electrode to be exposed is removed, and a  
18 region (B) where any parts other than said region (A) and said region (B)  
19 having a thickness smaller than that of said semiconductor layer;  
20 etching said semiconductor layer and said gate insulating  
21 film using said photoresist having said thickness in each part to expose  
22 said pixel electrode;  
23 removing at least said metallic layer located in upper side of  
24 said two layers in said exposed pixel electrode by etching process;  
25 removing said photoresist in said region (B) from upper side  
26 while leaving said photoresist in said region (A);  
27 removing said photoresist in any part other than that in said  
28 region (A); and  
29 forming a source/drain electrodes.

1 21. Method for manufacturing a TFT array of liquid crystal  
2 display comprising steps of:

3 depositing a gate electrode/gate line and a pixel electrode,  
4 each of said gate electrode/gate line and said pixel electrode including at  
5 least two layers comprising a transparent conductive layer and metallic  
6 layer provided on said transparent conductive layer, and subsequently  
7 etching said gate electrode/gate line and said pixel electrode using a

8 photoresist having a predetermined patterned shape corresponding to  
9 said gate electrode/gate line and said pixel electrode to form a  
10 predetermined patterns;

11 forming a gate insulating film and a semiconductor film;

12 forming a region (A) where at least of a portion of said  
13 photoresist corresponding to said semiconductor layer to be left has a  
14 thickness being larger than any other part of said photoresist, a region  
15 (C) where at least of a portion of said photoresist corresponding to a light  
16 transmitting part of said pixel electrode to be exposed is removed, and a  
17 region (B) where any parts other than said region (A) and said region (B)  
18 having a thickness smaller than that of said semiconductor layer;

19 etching said semiconductor layer and said gate insulating  
20 film using said photoresist having said thickness in each part to expose  
21 said pixel electrode;

22 removing said photoresist in said region (B) from upper side  
23 while leaving said photoresist in said region (A);

24 removing said photoresist in any part other than that in said  
25 region (A);

26 forming a source/drain electrode made of the same metallic  
27 material as that used for an upper layer of said two layers of said gate  
28 line; and

29 removing said source/drain electrode by etching process,  
30 while removing said metallic layer located in said upper layer of said two  
31 layers of said exposed pixel electrode by etching process.

1 22. TFT array substrate for a liquid crystal comprising:  
2 source lines and gate lines which are formed in matrix;

3 a pixel electrode for applying voltage to a liquid crystal and  
4 thin film transistors, said pixel electrode being provided in each of parts  
5 in which said source lines are intersected with said gate lines, said pixel  
6 electrode being protected by a passivation film;

7 a gate electrode;

8 a gate insulating film formed on said gate electrode;

9 a semiconductor layer film provided on said gate insulating  
10 film on a region of said gate electrode, said semiconductor layer being  
11 formed in such a manner as to contact with said gate insulating film;

12 a source electrode, a source line and a drain electrode, each  
13 of said source electrode, said source line and said drain electrode  
14 including at least two layers comprising a transparent conductive film  
15 and a metallic film provided on said transparent conductive layer, said  
16 transparent conductive film being formed in such a manner as to  
17 partially contact with said semiconductor layer;

18 wherein said drain electrode is connected with said pixel  
19 electrode by said transparent conductive layer per se;

20 wherein said passivation film, and said metallic film and said  
21 passivation film which are located on said light transmitting part of said  
22 pixel electrode are removed.

1 23. Method for manufacturing TFT array substrate for a  
2 liquid crystal display comprising steps of:

3 forming at least a gate insulating film and a semiconductor  
4 layer on a gate electrode;

5 forming a region (A) in a photoresist having a large thickness  
6 to be left as a semiconductor layer, a region (C) where a photoresist is

7 removed to expose a gate line, and a region (B) other than said region (A)  
8 in a photoresist having a thickness smaller than said region (A);

9 removing at least gate insulating film and said  
10 semiconductor layer which are located on said gate line by subjecting  
11 said gate insulating film and said semiconductor layer to etching  
12 process using a photoresist having different thickness to partially  
13 expose said gate electrode;

14 reducing the thickness of said photoresist, and subsequently  
15 removing said photoresist in said region (B) while leaving said  
16 photoresist in said region (A); and

17 removing said semiconductor layer located in a part other  
18 than said region (A).

1 24. Method for manufacturing a TFT array substrate  
2 comprising steps of:

3 depositing a conductive material for a gate electrode/gate  
4 line;

5 etching said deposited conductive material using a  
6 photoresist having patterned shape corresponding to said gate electrode  
7 and said gate line to form a predetermined patterns;

8 forming a gate insulating film and a semiconductor layer;

9 forming a region (A) in a photoresist having a large thickness  
10 to be left as a semiconductor layer, a region (C) where a photoresist is  
11 removed to expose a gate line, and a region (B) other than said region (A)  
12 in a photoresist having a thickness smaller than said region (A);

13 removing at least gate insulating film and said  
14 semiconductor layer which are located on said gate line by subjecting

15 said gate insulating film and said semiconductor layer to etching  
16 process using a photoresist having the above-mentioned shape to  
17 expose at least a part of said gate electrode;

18 removing said photoresist in said region (B) while leaving said  
19 photoresist in said region (A);

20 removing said semiconductor layer located in a part other  
21 than said region (A);

22 forming a source/drain electrodes using a photoresist having  
23 a patterned shape corresponding to said source/drain electrodes in a  
24 transparent conductive layer formed in such a manner as to partially  
25 contact with said semiconductor layer and a metallic layer formed on  
26 said transparent conductive layer;

27 forming a passivation film;

28 removing at least a light transmitting part of said passivation  
29 film over a pixel electrode; and

30 forming a pixel electrode by removing said metallic layer on  
31 said transparent conductive layer from said removed passivation film  
32 formed on said pixel electrode.

1 25. The thin film transistor array substrate according to any  
2 one of claims 1, 12, 13, 14, 15, 16 or 22, wherein a semiconductor  
3 pattern is formed to have a region surrounding a thin film transistor and  
4 a region surrounding a source electrode and at least a part of a source  
5 line, and at the source electrode part in a pixel region, a part of the  
6 semiconductor pattern surrounding the source electrode exists only on a  
7 gate line.

1           26. The method of manufacturing a thin film transistor array  
2 substrate according to any one of claims 17, 18, 19, 20, 21, 23 or 24  
3 wherein a semiconductor pattern is formed to have a region surrounding  
4 a thin film transistor and a region surrounding a source electrode and at  
5 least a part of a source line, and at the source electrode part in a pixel  
6 region, said semiconductor pattern is formed so that a part of the  
7 semiconductor pattern surrounding the source electrode exists only on a  
8 gate line.

1           27. A liquid crystal display apparatus comprising a thin film  
2 transistor array substrate manufactured by the method according to  
3 any one of claims 6, 7, 8, 9, 10, 17, 18, 19, 20, 21, 23 or 24.

1           28. A liquid crystal display apparatus comprising a thin film  
2 transistor array substrate according to any one of claims 1, 2, 3, 4, 5, 8,  
3 11, 12, 13, 14, 15, 16 or 22.